AN INVESTIGATION OF TRANSISTORS AS VOLTAGE MULTIPLIERS

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Submitted to the Department of Naval Architecture and Marine Engineering on May 16, 1952 in partial fulfillment of the requirements for the degree of Naval Engineer.

ABSTRACT

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Submitted to the Department of Naval Architecture and Marine Engineering on May 16, 1952 in partial fulfillment of the requirements for the degree of Naval Engineer.

The object of this thesis is to find out how well the function of voltage multiplication can be accomplished through the use of presently available transistors.

The problem is analyzed by expressing, in a Taylor Series, the collector current as a function of the inputs (collector voltage and emitter current). Through analysis of the resulting series for sinusoidal inputs, the component of collector current at the sum or difference of the input frequencies is separated as

$$I_c = (a_5 + a_{12}V_c^2 + a_{14}I_\varepsilon^2)\, V_c I_\varepsilon.$$

These coefficients were experimentally determined for a standard Western Electric, Type A-1698, transistor and a General Electric, Type 11, transistor on which the point-contact pressure had been lightened and to which

an external resistive network had been added. An attempt was made to maximize the coefficient a_{13} and to minimize a_{12} and a_{14}. The variations of these coefficients as a function of frequency were determined for the modified General Electric transistor described above.

At a specific operating point, with input frequencies of 350 cps and 450 cps, and with variations of E_c up to 0.65 volt rms and I_ε up to 0.2 milliampere rms, the Western Electric transistor exhibited a maximum error of 5 percent from ideal multiplication. At the same operating point and with the same frequencies, the modified transistor had 5 percent maximum error within a range of E_c up to 2.5 volts rms and I_ε up to 1.0 milliampere rms. The modified transistor exhibited a useful upper limit of input frequencies of approximately 10 kc.

It is recommended that further investigation be undertaken to determine the effects upon the range and accuracy of multiplication brought about by variations of the operating points of both transistors, by changes in the resistive network of the General Electric transistor, by changes in operating temperature, and by interchanging transistors of the same type.

Thesis Supervisor: J. Francis Reintjes
Title: Assistant Professor of Electrical Communications

Cambridge, Massachusetts
May 16, 1952

Professor Leicester F. Hamilton
Assistant Secretary of the Faculty
Massachusetts Institute of Technology
Cambridge, Massachusetts

Dear Sir:

In accordance with the requirements for the degree of Naval Engineer, we submit herewith a thesis entitled "An Investigation of Transistors as Voltage Multipliers".

Respectfully,

ACKNOWLEDGMENTS

The authors wish to acknowledge their indebtedness to Professor J. F. Reintjes for his advice and encouragement throughout the accomplishment of this investigation. They also wish to express their appreciation to Professor R. B. Adler for his constructive criticisms. The authors acknowledge at this time that, to the best of their knowledge, it was Mr. Carl Hurtig, attached to the M.I.T. Electronics Research Laboratory, who first found that reducing the point-contact pressure of a transistor could measurably straighten the constant i_e curves shown on the collector characteristics.

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I. INTRODUCTION

Because multiplication of two electrical signals, either voltages, currents, or a combination of the two, is an important operation in most electrical computation, many schemes have been devised to yield an output proportional to the product of the inputs. It is the purpose of this thesis to investigate the suitability of transistors for this operation.

The methods of multiplication can be roughly divided into frequency bands over which they are applicable. For instance, in the low frequency range, up to about 100 cps, many purely mechanical methods are available. One of the most accurate and best known methods is that employed by Bush and Caldwell[1], which utilized the wheel and disc integrator. The product of x and y was formed in accordance with the equation: $xy = \int x\,dy + \int y\,dx$. The error of this method probably would not exceed one part in 25,000, but the equipment is very expensive.

A number of other mechanical methods are available. Among these are logarithmic cams, mechanical models of similar triangles, and various types of bar-linkages[2]. These devices, while slightly faster than the integrator method, are also strictly limited as to frequency, and have a probable error of from 0.1 to 1 percent.

Also in the low frequency range, combination mechanical and electrical methods, utilizing servo driven bridges and potentiometers, have been used[3]. These devices have an error of about 0.1 percent.

An electronic pulse method has been used in which one input controls the amplitude of a rectangular wave, and the other input controls the duty ratio[4]. The time integral of the wave is proportional to the product of the two inputs. This scheme yields an error of less than 1 percent, but is limited in frequency to about 60 cps.

In a medium frequency range, up to about 1 kc, the simple electrodynamometer and a probability method have been used. The electrodynamometer operates on the principle that when two fluxes surrounding a fixed and movable coil are each made proportional to an input voltage, the resultant torque is proportional to the product of the two input voltages. The probability method, devised by Hardy[3], is based on the fact that the probability of time coincidence of pulses occurring at noncommensurable rates is proportional to the products of the probabilities of the occurrence of the separate pulses at a given time. The input quantities control the duty ratios of the various pulse sources, while the duty ratio of the output of a coincidence circuit gives a measure of the product of the quantities. An

error of less than 4 percent has been obtained by this method.

Various purely electronic devices may be used to perform multiplication for frequencies up to about 50 kc.

Selected high-vacuum tubes with square-law characteristics have been utilized in this range(5). The two voltages, e_1 and e_2, to be multiplied are added and fed into the square-law tube. This yields $e_1^2 + 2e_1e_2 + e_2^2$. Simultaneously the two voltages are subtracted and fed into another square-law tube which yields $e_1^2 - 2e_1e_2 + e_2^2$. By subtracting the second of these results from the first, a product term, $4e_1e_2$, is obtained. Obviously any variation from perfect square-law characteristics in the tubes will cause error terms to arise. Balancing circuits have been designed to minimize such variations caused by aging, temperature changes and drift due to random fluctuations of the tube emission(6). In this manner, errors of less than 0.5 percent have been obtained. A disadvantage of this type circuit is the difficulty of separating the product (including the d-c component of the product) from the plate supply voltage.

The use of germanium crystal rectifiers in a voltage range where they have approximately square-law characteristics largely overcomes drift difficulties. An additional advantage is that the input capacitance of these rectifiers is about one tenth that of the square-law

tubes. However, the input transformer required to form the sum and difference of the inputs must also step down the input impedance to match the low impedance of the crystals. The product is then of very low voltage but does not require separation from the plate supply voltage, as was the case for the vacuum tubes. These rectifiers also exhibit hysteresis effects, and are not readily interchangeable because of large variations from the manufacturer's characteristics. Thus this use of crystal rectifiers shows little advantage over a similar use of vacuum tubes.

Exponential-law devices which use transfer characteristics of remote cut-off pentodes, current-voltage characteristics of high vacuum diodes in the negative plate voltage region, and copper-oxide or germanium rectifier bridges have been investigated by others[3,7]. These devices have been designed with an error of less than 2 percent, but they exhibit the same difficulties as the square-law devices previously discussed. An exponential-law method utilizing the principle of discharging capacitors has also been investigated[3]. The accuracy was about four times better than the types mentioned above. However, this device is limited in frequency to about 2 kc due to the time required for discharge of the capacitors.

A carrier-frequency multiplier has also been devised which makes use of a variable gain amplifier, the gain of which is controlled in accordance with one input signal by means of a feedback loop[3]. The amplifier input is the other signal. Thus the output is proportional to the product of the two inputs. This multiplier has an upper frequency limit of about 50 kc. It is the fastest device mentioned.

Multiplication methods which use multi-electrode vacuum tubes have utilized[9]. The converter tube has the property that its plate current is proportional to the product of the input voltages applied to the two control grids. The inputs must be unidirectional, therefore alternating inputs must be suitably biased. The important disadvantage of the converter tube as a multiplier is the difficulty of separating the desired product from the plate supply circuit. This difficulty can be overcome by using a tuned transformer, provided that one of the inputs is modulated prior to its application to the multiplier. The product is now shifted in frequency by the amount of the carrier and is readily amplified in a a-c coupled amplifier. The sense (positive or negative) of the product is determined by its phase with respect to the carrier.

The input applied via the modulator appears in the plate circuit and passes through the plate-circuit tuned

transformer along with the product term. This input term is undesired, and although it lies outside the frequency range of the desired product term, it may be much larger in amplitude. The output of the desired term may therefore be limited by overloading due to this undesired term.

If both of the inputs were modulated, the product can be selected by means of a filter tuned to the sum or difference frequency of the two carrier input frequencies. There is then no undesired term at a high level in the output of the multiplier. Overloading and limitation of the output by the undesired term is thus avoided. The relative disadvantage of this scheme is the increased equipment required.

The example methods mentioned above far from complete the many ways in which electronic signal multiplication has been accomplished. They do, however, indicate the scope of the problem.

It can be shown that any nonlinear device, having an output which is a function of two variables, will exhibit in its output a sum or difference frequency term, a portion of which is proportional to the product of the two variables. The rest of that term can be considered as an error. If the error is small enough, multiplication can be nicely accomplished using a modulation scheme similar to that employed with the converter tube described

above. Bowers[10], working with a transistor, has isolated this term. He has found that over a very limited dynamic range, the error portion is relatively small. In order to find out how well a transistor can accomplish the function of a converter tube, this investigation has set out to determine this error portion, and to attempt to find means of minimizing it.

II. PROCEDURE

In this section the essential steps followed to obtain the final useful data are described. Details of these steps are presented in the Appendix, pages 32 to 42. Also presented in the Appendix are the investigations carried out, but later discontinued because they led either to inconclusive or inadequate information.

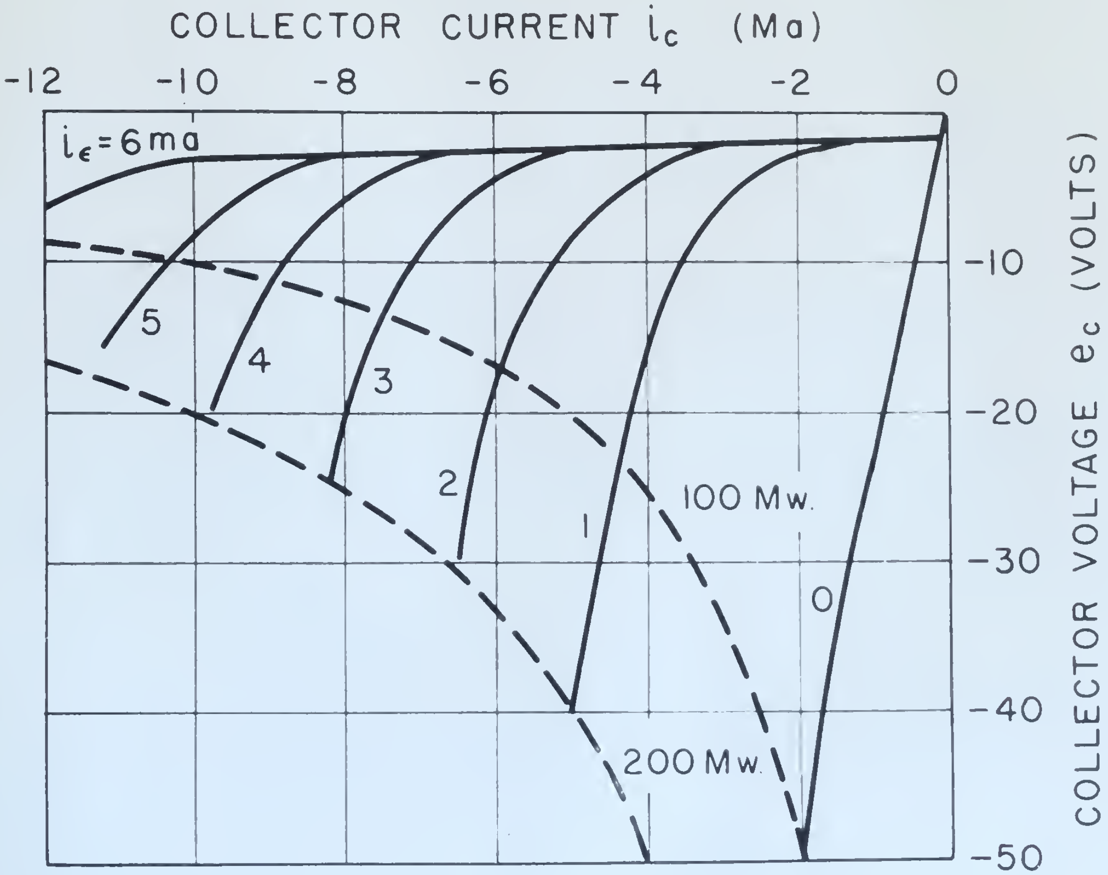
In all the following work, the symbolism as indicated below has been used; lower-case letters stand for instantaneous values, upper-case letters for rms values of sinusoidally varying quantities, upper-case letters with subscript "m" for peak values of sinusoidally varying quantities and upper-case letters with subscript "o" for direct values.

Two investigations were carried out simultaneously. In one study the application of a commercial Western Electric, Type A-1698, transistor to multiplication was investigated. In the other study an adjusted General Electric, Type 11, transistor was investigated along the same lines.

A typical set of collector voltage (e_c) versus collector current (i_c) characteristics are shown in Figure 1. From an examination of the collector characteristics it was decided that the most feasable type of multiplication would be that of multiplying collector

FIGURE I

MANUFACTURER'S CHARACTERISTICS OF
WESTERN ELECTRIC TRANSISTOR
MODEL A 1698



voltage times emitter current, and taking collector current as the output. Since the transformation of currents to voltages and vice verse is a simple operation, the end result of multiplying voltages and getting a voltage proportional to the product is still retained.

It follows that for ideal multiplication, the collector characteristics should be such that the curves of constant emitter current (i_ε) are radial straight lines emanating from the origin. Also, at constant collector voltage, the incremental values of collector current for equal incremental values of emitter current are constant. To show this:

If $i_c = K\, e_c\, i_\varepsilon$

for $i_\varepsilon = c_1$

$i_c = K\, c_1\, e_c.$

This shows that the constant i_ε curves are straight lines from the origin.

For $e_c = c_2$

$i_c = K\, c_2\, i_\varepsilon.$

This shows that increments of collector current are constant for equal increments of emitter current.

For any general characteristics, operation can be visualized from an inspection of a Taylor Series expansion of i_c as a function of i_ε and e_c about an operating point. This complete expansion is shown in the Appendix, pages 38 to 42, for two sinusoidal inputs of different frequencies.

It is seen from this expansion that the term containing the sum and difference of the input frequencies has a component that is proportional to the product of the amplitudes of the inputs. But it also contains components which are proportional to other functions of the inputs; these are error components.

Mathematically:

$$I_c \begin{pmatrix}\text{sum or}\\ \text{difference}\\ \text{frequency}\end{pmatrix} = a_5 E_c I_\varepsilon + a_{12} E_c^3 I_\varepsilon + a_{14} E_c I_\varepsilon^3 + a_{22} E_c^2 I_\varepsilon^4 + a_{23} E_c^3 I_\varepsilon^3 + a_{24} E_c^4 I_\varepsilon^2 + \cdots\cdots$$

It was found that, within the accuracy of the measurement devices employed, only the first three terms of the above equation were of sufficient magnitude to be measurable. If the fourth and subsequent terms are ignored, this equation becomes:

$$I_c \begin{pmatrix}\text{sum or}\\ \text{difference}\\ \text{frequency}\end{pmatrix} = a_5 E_c I_\varepsilon + a_{12} E_c^3 I_\varepsilon + a_{14} E_c I_\varepsilon^3 \qquad (1)$$

where
$$a_5 = \left.\frac{\partial^2 i_c}{\partial i_\varepsilon\, \partial e_c}\right]_{I_{co}}$$

$$a_{12} = \left.\frac{\partial^4 i_c}{\partial e_c^3\, \partial i_\varepsilon} \times \frac{1}{4}\right]_{I_{co}}$$

$$a_{14} = \left.\frac{\partial^4 i_c}{\partial e_c\, \partial i_\varepsilon^3} \times \frac{1}{4}\right]_{I_{co}}$$

For convenience the dimensions of the quantities used are in volts and milliamperes.

Note that the complete expression, in the Appendix on page 41, indicates that for ideal multiplication, a_4, a_6 and all the following coefficients must be zero, thereby yielding the straight line characteristics described above. If that portion of the output (I_c) that is at the sum or difference frequency of the inputs (E_c and I_ε) is isolated, perfect incremental multiplication would result if a_{12}, a_{14}, and succeeding coefficients contributing to the sum or difference frequency portion vanished. Therefore one desired result was a determination of a_5, a_{12} and a_{14}. A second desired result was a means of maximizing a_5 and minimizing a_{12} and a_{14}.

As part of one investigation the point-contact pressure of a General Electric, Type 11, transistor was reduced. This had the fortuitous result of measurably straightening the constant i_ε curves shown on the collector characteristics. It was further known that adjustment of the padding resistors shown in Figure II would have marked effects upon the characteristics of the equivalent transistor, where the equivalent transistor is now considered to be that inside the terminals.

Interdependent adjustments of R_1, R_2 and R_3 were made until the characteristics of the equivalent transistor, about the operating point $V_{co} = -4$ volts, $I_{\varepsilon o} = 1.5$ ma, were apparently the best obtainable in regard to radial linearity and equal horizontal spacing.

The two investigations measured the coefficients a_5, a_{12} and a_{14} by means of the circuits shown in Figures III and IV. For one investigation the whole of Figure II was inserted within the four terminals shown in Figure III. For the other, Figure IV was used as shown. The I_c and I_ε inputs were varied and the I_c output was measured at $\omega_2 - \omega_1 = 100$ cps, at $3\omega_1 + \omega_2 = 1500$ cps, and at $3\omega_2 - \omega_1 = 1000$ cps. Measurements at the last two frequencies were used to calculate the magnitudes of a_{12} and a_{14}. The signs of these coefficients were determined from a consideration of the change in slope of the output, holding one input constant and increasing the other. Sample calculations are shown in the Appendix, page 43 .

The expression thus obtained for the output current was compared with the measured values for overall accuracy. The dynamic range of multiplication was determined for a maximum error of 5 percent.

The range of possible input frequencies of the modified, padded transistor of Figure II, was investigated by means of the circuit of Figure III, while maintaining the order of magnitude of the difference frequency. The multiplier output was measured as a function of the mean of the input frequencies. The accuracy of multiplication was determined for these higher frequencies.

FIGURE II

EQUIVALENT TRANSISTOR

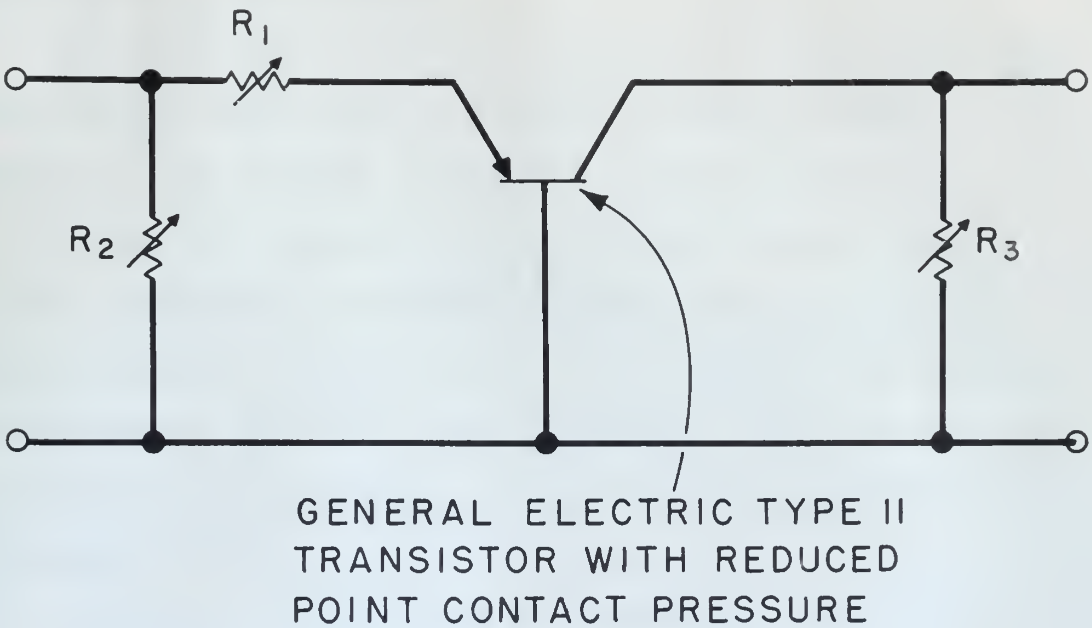
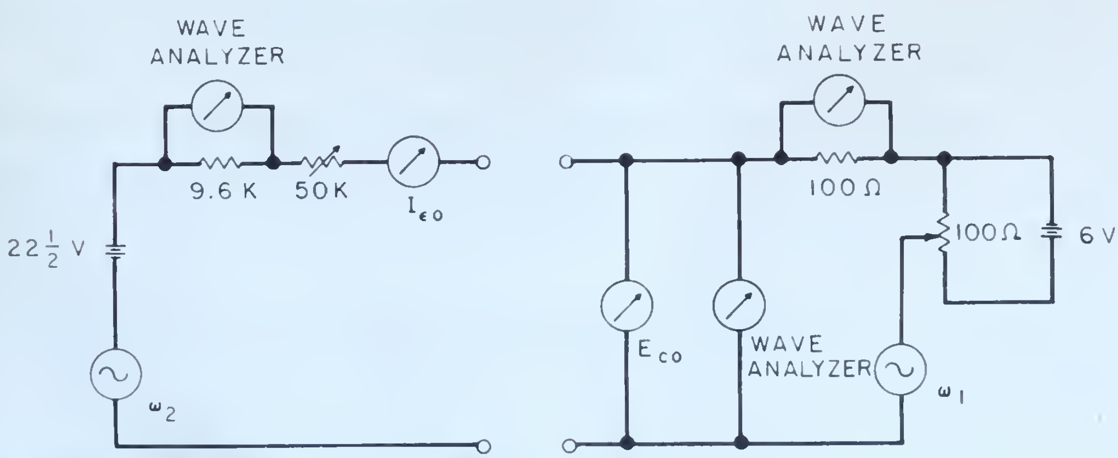


FIGURE III

MEASURING CIRCUIT FOR DIFFERENCE FREQUENCY CURRENT



BIAS: $E_{co} = -4$ v

$I_{\epsilon o} = 1.5$ ma

III. RESULTS

Type A-1698 Investigation

The difference frequency component of the output (i_c) was measured while using a standard, unpadded Western Electric, Type A-1698, transistor in the circuit of Figure IV. The observed data is plotted on Figures V and VI. Indicated on Figure V is the area of operation within which the maximum error of the output from perfect multiplication was less than 5 percent. The coefficients of equation (1) on page 11 were calculated yielding the following result:

$$I_c \text{ (sum or difference frequency)} = (0.31[illegible] - 0.0377\, E_c^2 - 0.350\, I_\varepsilon^2)\, E_c I_\varepsilon \quad (2)$$

This equation defines the measured data out to $E_c = 1.5$ volts within an accuracy of 1 percent.

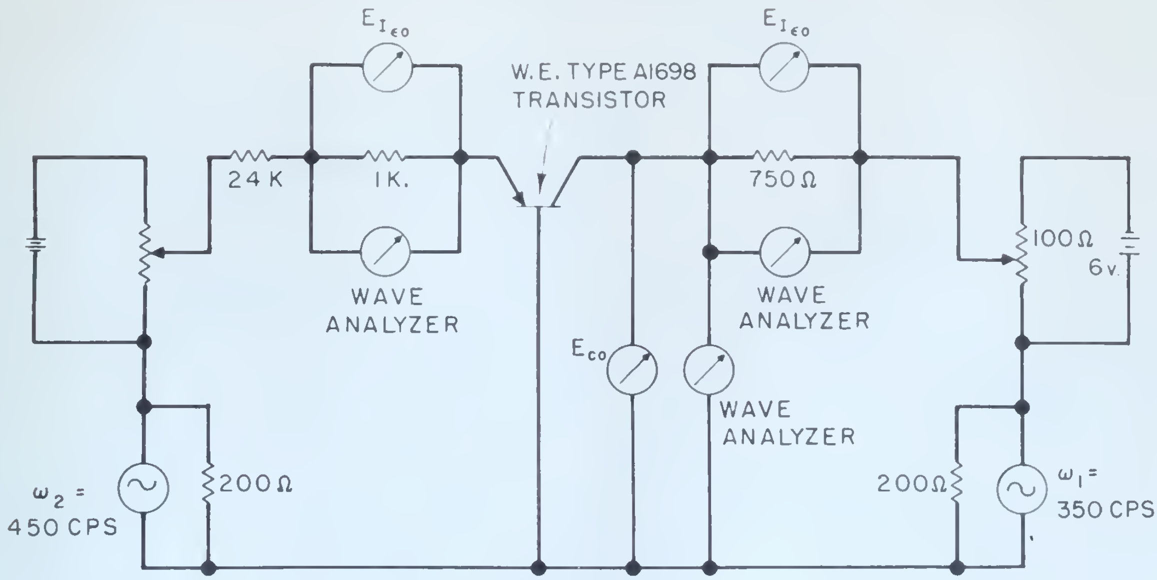
Adjustment of Resistive Padding with Type 11

The changes in the collector characteristics of the equivalent transistor caused by varying the resistances shown in Figure II were investigated.

R_1

Decreasing R_1 fanned the curves of constant i_ε clockwise. The movement was not uniform. The $i_\varepsilon = 0$ curve remained relatively stationary as did the high i_ε curves which were nearly horizontal. This adjustment had little

FIGURE IV
MEASURING CIRCUIT FOR DIFFERENCE FREQUENCY CURRENTS



BIASES $E_{co} = -4$ v.
$I_{\epsilon o} = 1.5$ ma

FIGURE V

EXPERIMENTAL DIFFERENCE FREQUENCY OUTPUT CURRENT VS INPUTS APRIL 15, 1952 R. G. I.

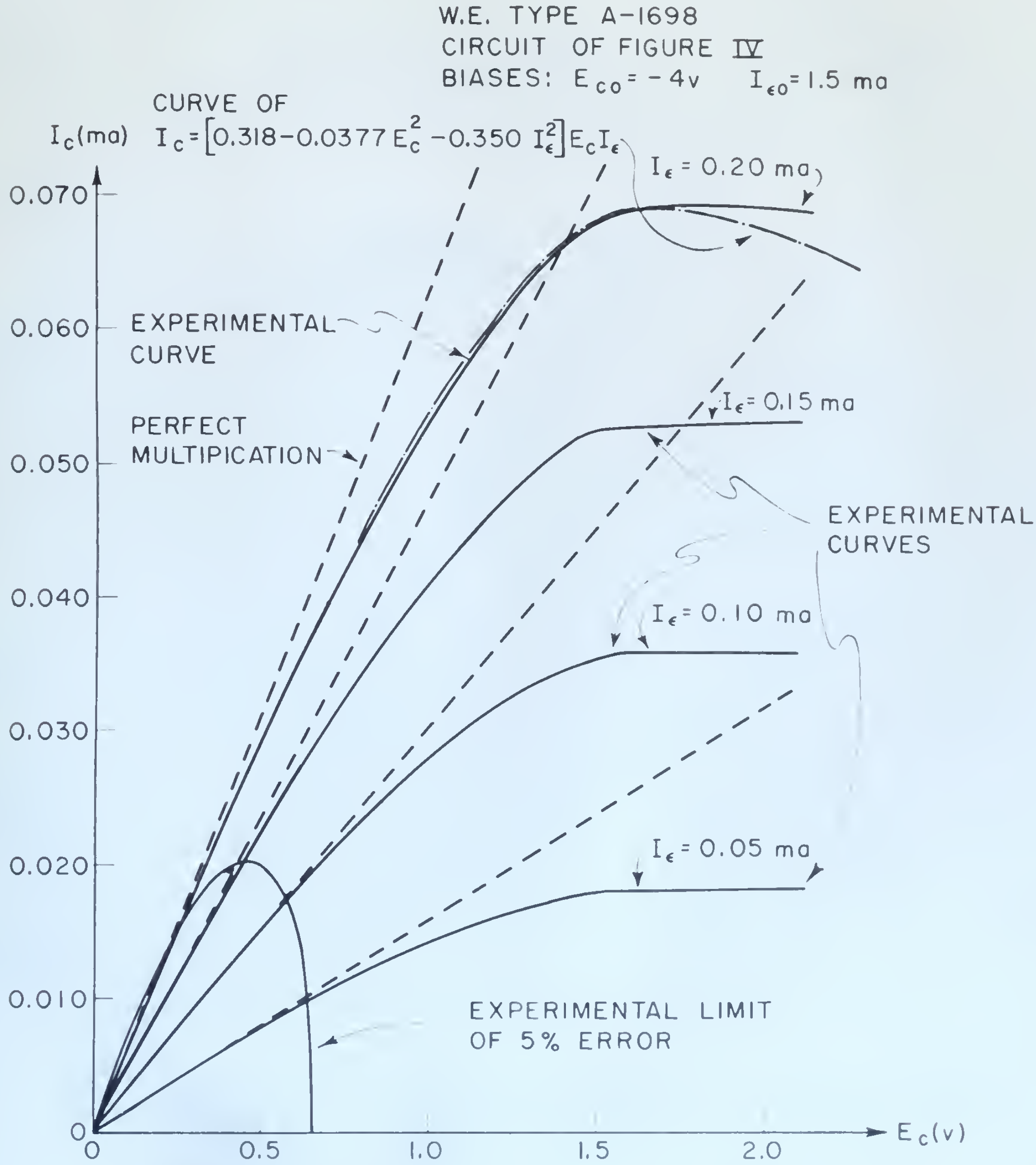
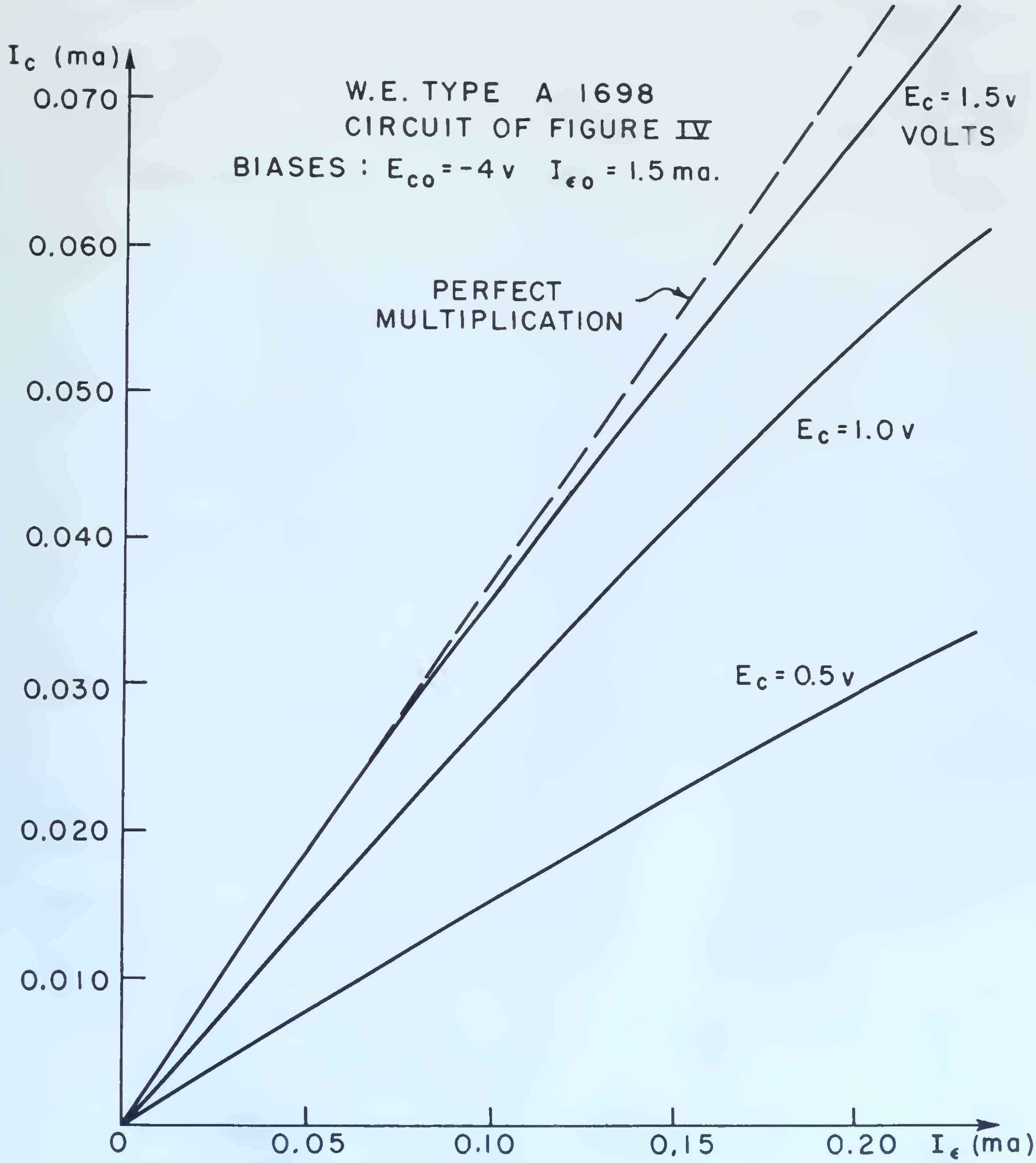


FIGURE VI

EXPERIMENTAL DIFFERENCE FREQUENCY OUTPUT CURRENT VS. INPUTS (CROSS CURVE) APRIL 15, 1952
R.G.I.



effect upon the linearity, but the horizontal spacing was measurably changed.

$\underline{R_2}$

Decreasing R_2 had a contrasting effect from that observed with a similar adjustment of R_1. The constant i_ε curves were fanned counter-clockwise. As with R_1, the $i_\varepsilon = 0$ and high i_ε curves remained relatively stationary. This adjustment also primarily effected the horizontal spacing.

$\underline{R_3}$

Decreasing R_3 fanned all the constant i_ε curves clockwise. Again the movement was not uniform. The higher i_ε curves merged together more quickly than the lower curves. The linearity of the curves increased as R_3 was decreased.

Optimum settings of these resistors were found to be approximately: $R_1 = 400\Omega$, $R_2 = 750\Omega$ and $R_3 = 5{,}000\Omega$.

<u>Low Frequency Investigation of Padded Type 11</u>

The General Electric, Type 11, transistor with reduced point-contact pressure and padded with the resistance values determined above, was inserted in the circuit of Figure III. The difference frequency component of the output (I_c) was measured and is plotted on Figures VII and VIII. Indicated on Figure VII is the area of operation within which the maximum error of the output from perfect multiplication was less than 5 percent. The coefficients of equation (1) on page 11 were calculated yielding the

FIGURE VII

EXPERIMENTAL DIFFERENCE FREQUENCY OUTPUT CURRENT VS INPUTS
APRIL 4, 1952 S.N.R.
G. E. MODIFIED, PADDED TYPE II
CIRCUIT OF FIGURE III

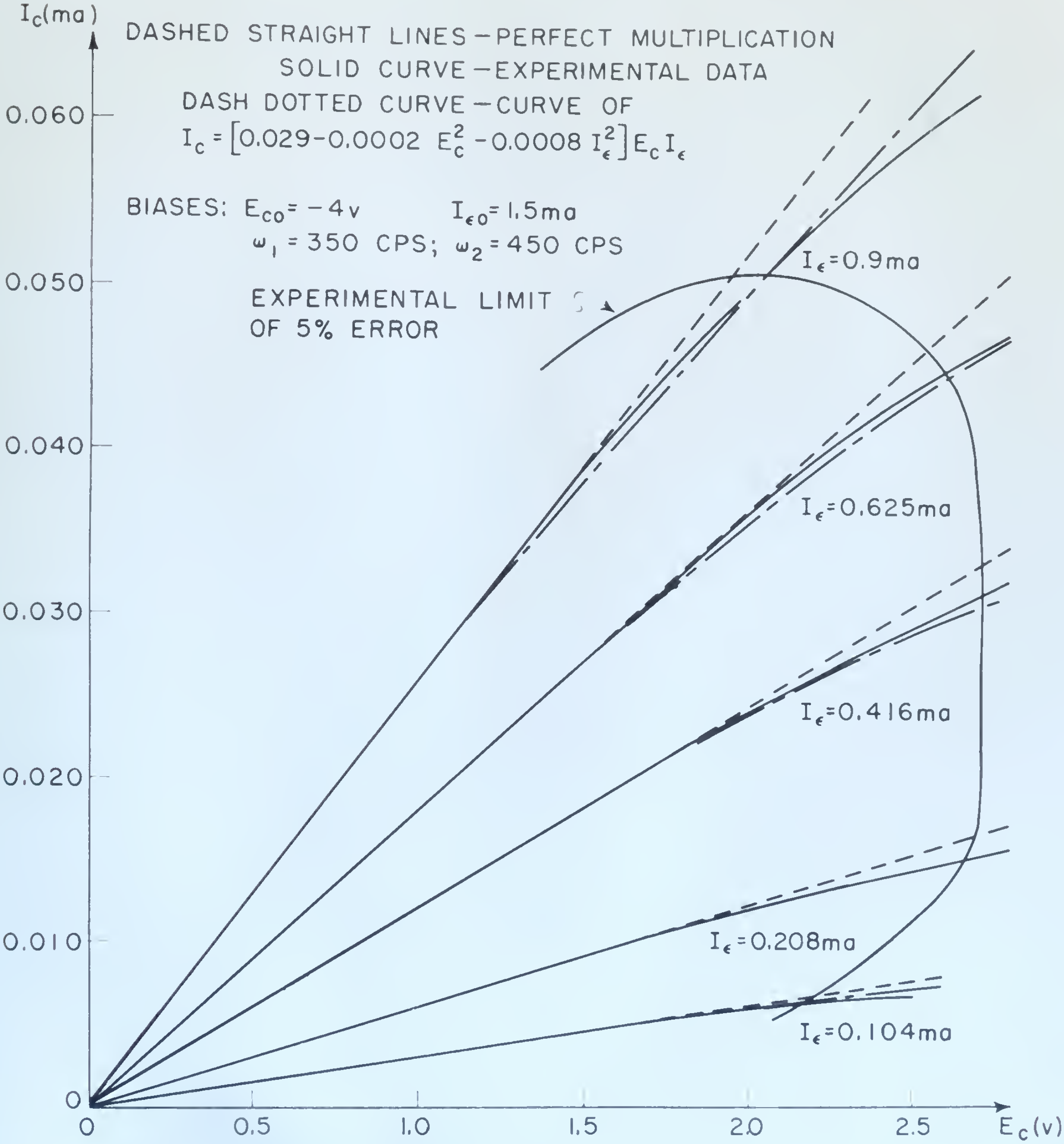
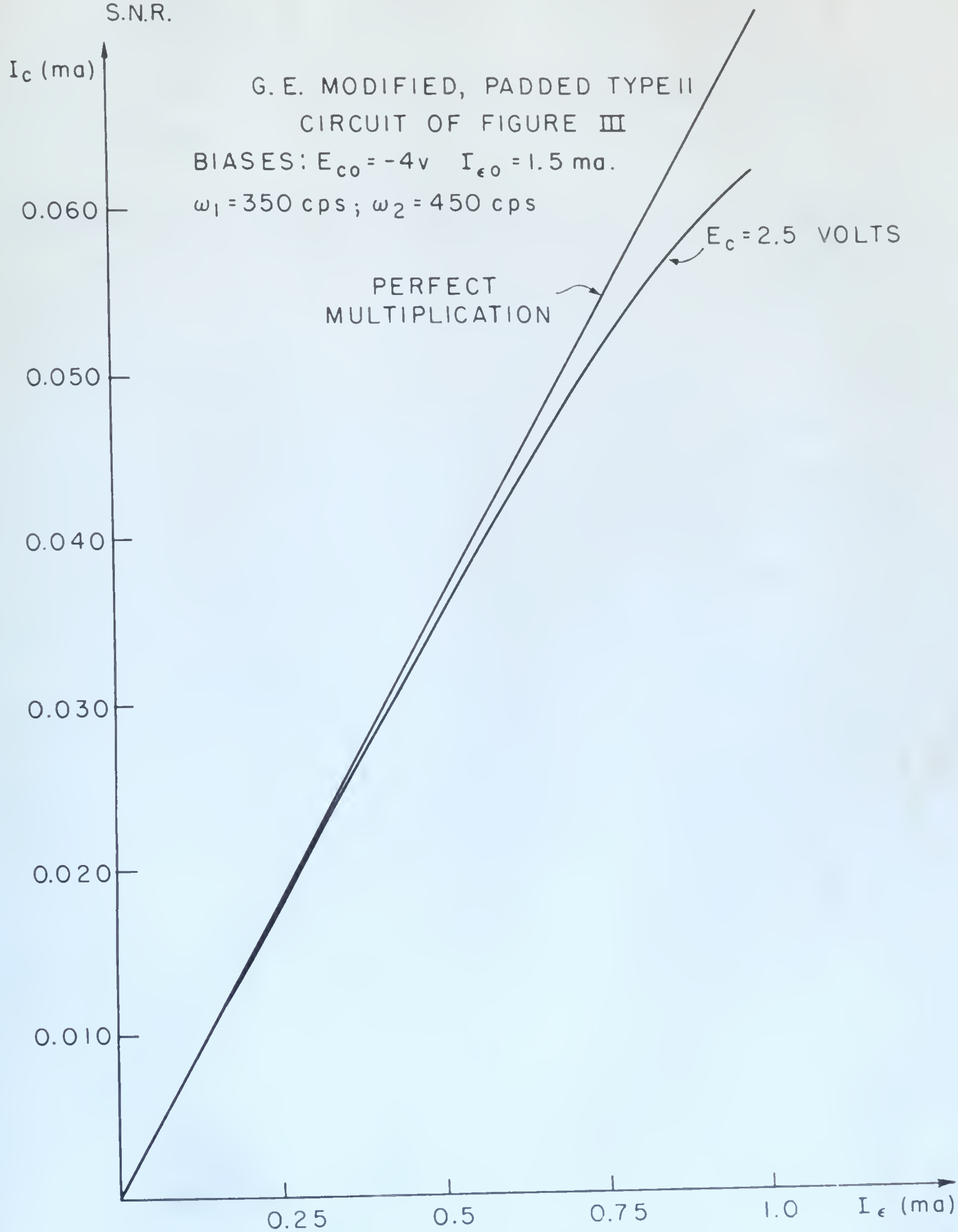


FIGURE VIII

EXPERIMENTAL DIFFERENCE FREQUENCY OUTPUT CURRENT VS. INPUTS (CROSS CURVE) APRIL 4, 1952
S.N.R.



following result:

$$I_c \text{ (sum or difference frequency)} = (0.029 - 0.0002\, E_c^2 - 0.0008\, I_\varepsilon^2)\, E_c\, I_\varepsilon \quad (3)$$

This equation defines the measured data within an accuracy of 3 percent.

<u>Response as a Function of Frequency of the Radded Type 11</u>

The values of ω_1 and ω_2 were varied in the circuit of Figure III. The sum or difference frequency component of the output (i_c) was measured and is plotted on Figure IX for I_ε = 0.208 ma, and on Figure X for I_ε = 0.416 ma. Figure XI was derived from Figures IX and X by choosing a constant E_c of 1 volt and plotting the difference frequency component of the output versus the mean of the input frequencies for the two emitter currents shown.

The coefficients of equation (1), as a function of frequency, were determined by trial and error to make this equation most nearly fit the data plotted in Figures IX and X. These coefficients are plotted on Figure XII.

FIGURE IX

EXPERIMENTAL DIFFERENCE FREQUENCY OUTPUT CURRENT VS. INPUTS APRIL 25, 1952 S.N.R., R.G.I.

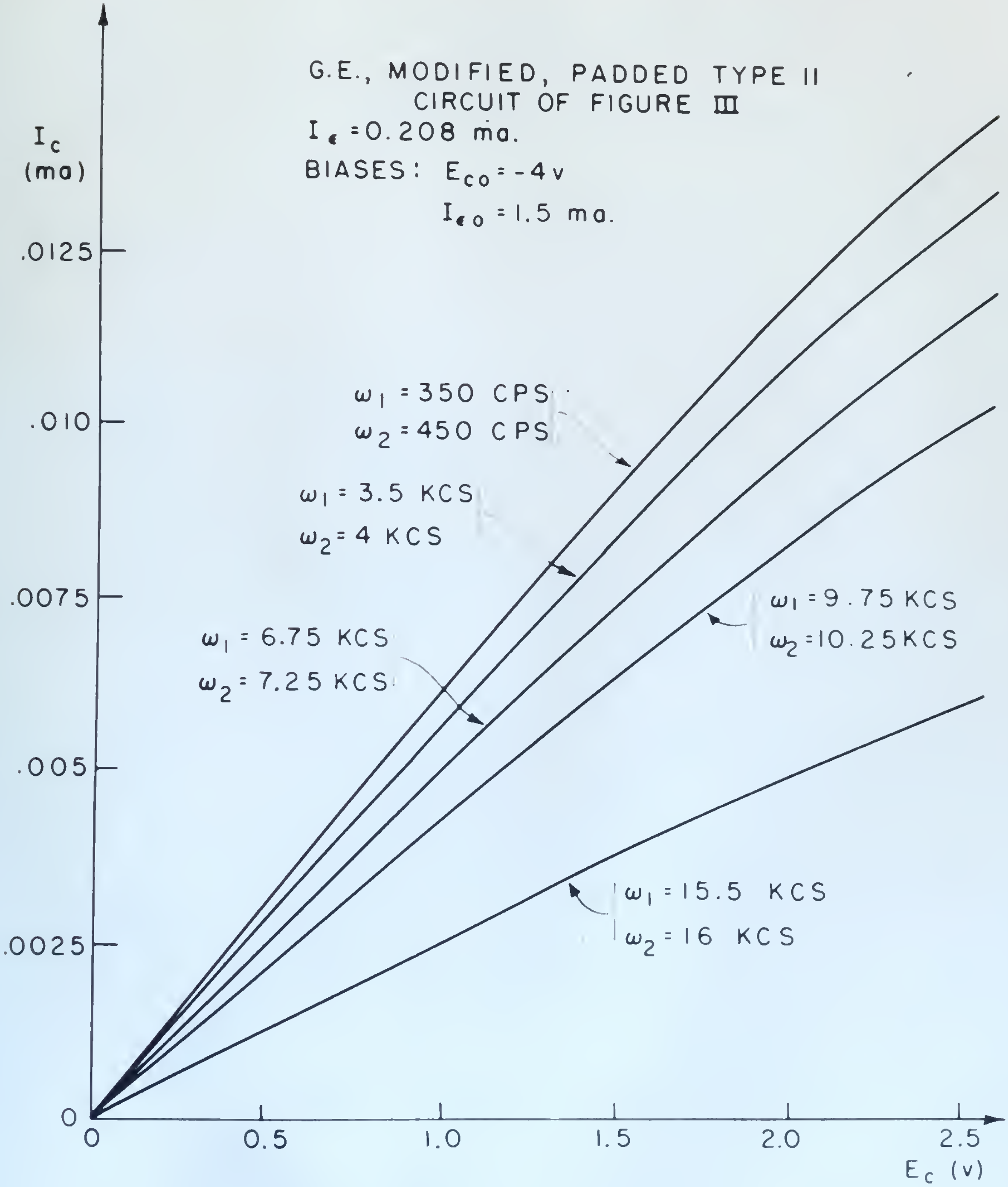


FIGURE X

EXPERIMENTAL DIFFERENCE FREQUENCY OUTPUT CURRENT VS INPUTS APRIL 25, 1952 S.N.R. R.G.I.

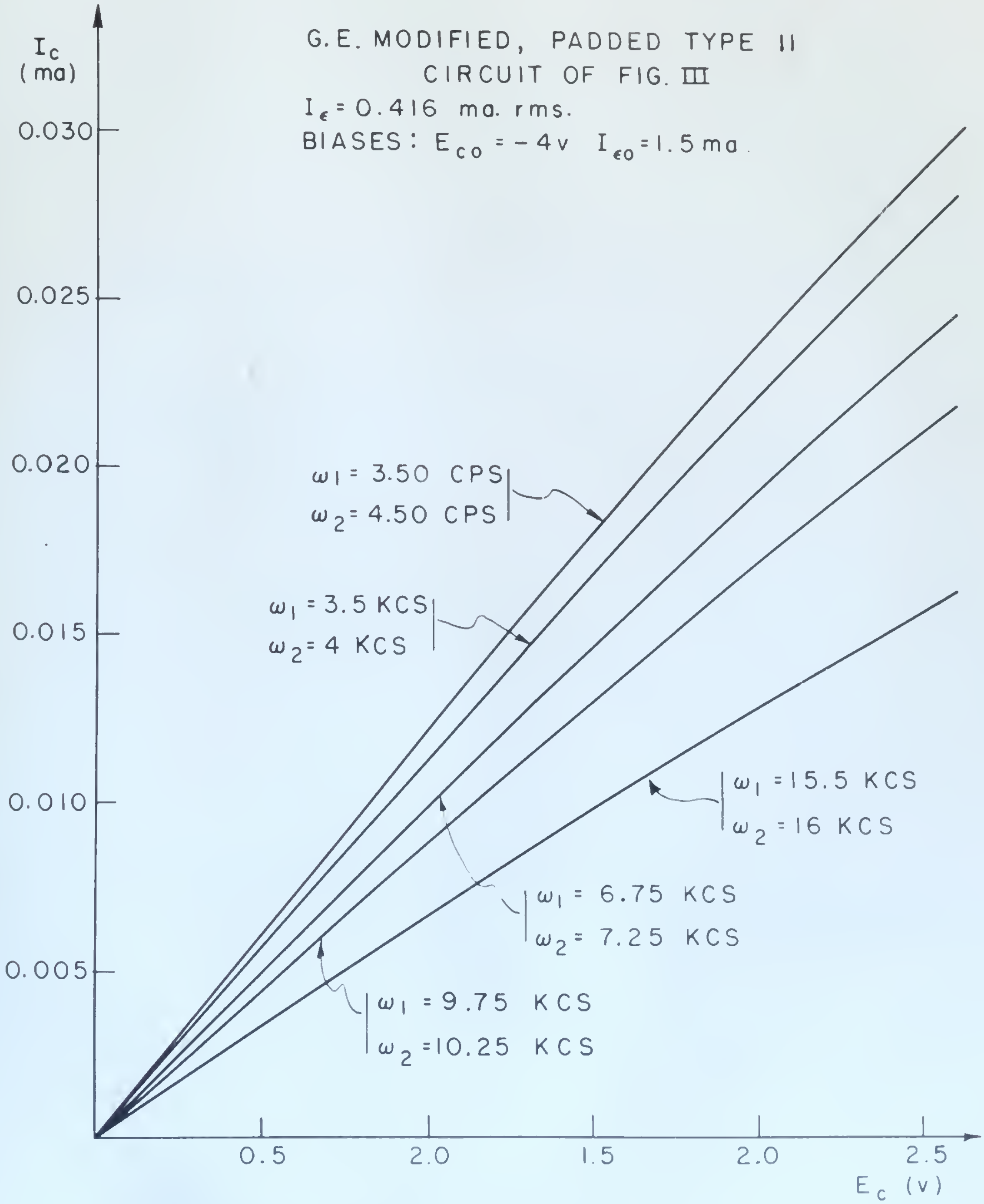


FIGURE XI

EXPERIMENTAL DIFFERENCE FREQUENCY OUTPUT CURRENT VS FREQUENCY
APRIL 25, 1952 SNR RGI

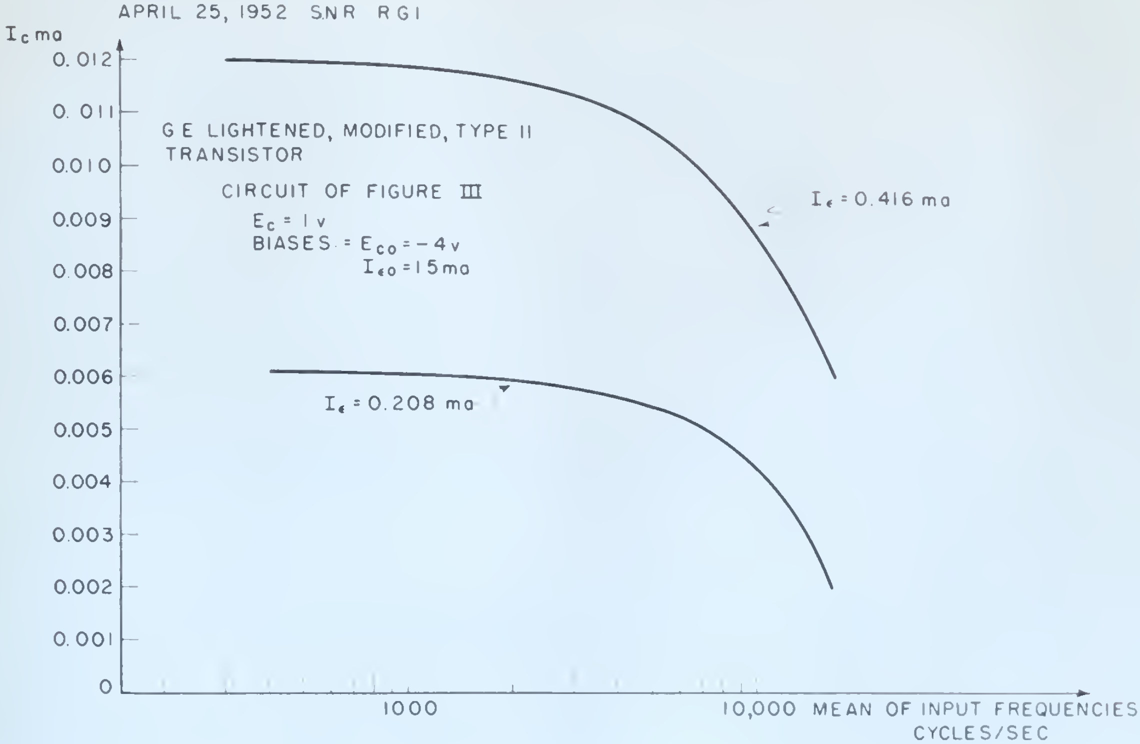
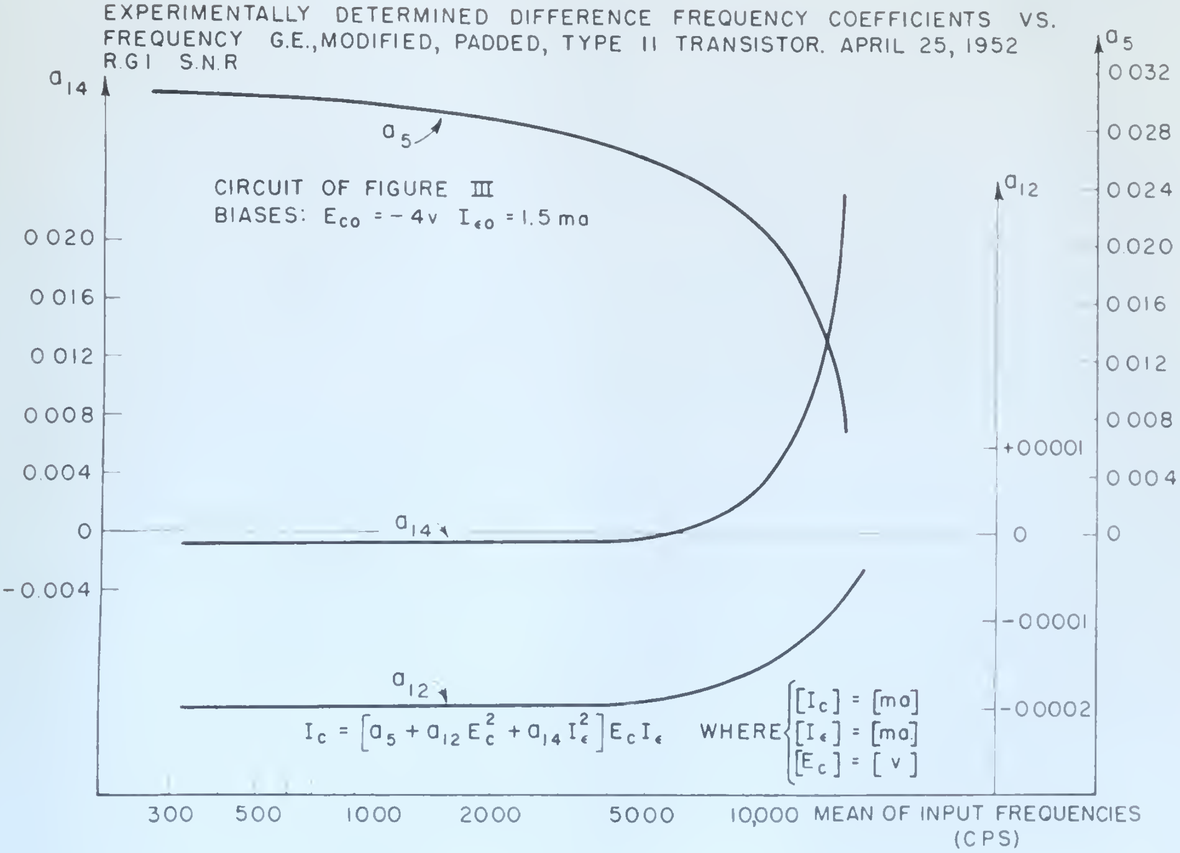


FIGURE XII

EXPERIMENTALLY DETERMINED DIFFERENCE FREQUENCY COEFFICIENTS VS. FREQUENCY G.E., MODIFIED, PADDED, TYPE 11 TRANSISTOR. APRIL 25, 1952
R.G.I S.N.R



IV. DISCUSSION OF RESULTS

Optimum Adjustment of Operating Point

For comparison purposes the biases of the standard Western Electric, Type A-1698, transistor were arbitrarily set at $V_{co} = -4$ v and $I_{eo} = 1.5$ ma. It was felt that the transistor operation as a multiplier was not too sensitive to changes in the applied biases. However, since no investigation of various operating points has been made, it cannot be definitely concluded that the chosen operating point gives the maximum range or accuracy of multiplication. Because of this indecision, it is recommended that further investigation be undertaken at different biases to determine the optimum operating point.

The operating point and padding resistance values used with the modified General Electric, Type 11, transistor were determined for the approximate maximum accuracy of multiplication. The procedure used is discussed in detail in the Appendix on pages 36 to 38. In this instance, it was felt that near maximum accuracy was attained. It is conceivable, however, that this setting did not yield a corresponding maximum range of inputs; considering the upper limit to be fixed by acceptable accuracy, and the lower limit to be fixed by noise. It is therefore felt that further investigation of maximum accuracy and range of inputs should be undertaken. This could be accomplished

by first varying the applied biases, then adjusting the padding resistances as already described, and finally analyzing the difference frequency component of the output for range and accuracy.

Comparison Between Outputs of Types 11 and A-1698

For comparing the accuracy and range of multiplication between the two proposed transistor components, both the graphical presentation of Figures V and VII and the equations (2) and (3) will be utilized. For ready reference these equations are:

$$I_c = (0.318 - 0.0377\, E_c^2 - 0.350\, I_\varepsilon^2)\, E_c\, I_\varepsilon \qquad (2)$$

for the standard Western Electric, Type A-1698, transistor, and

$$I_c = (0.029 - 0.0002\, E_c^2 - 0.0008\, I_\varepsilon^2)\, E_c\, I_\varepsilon \qquad (3)$$

for the padded, modified contact pressure, General Electric, Type 11, transistor.

Normalizing these equations with respect to the input product yields for equation (2)

$$\frac{I_c}{0.318} = (1 - 0.1185\, E_c^2 - 1.1\, I_\varepsilon^2)\, E_c\, I_\varepsilon ,$$

and for equation (3)

$$\frac{I_c}{0.029} = (1 - 0.0069\, E_c^2 - 0.0276\, I_\varepsilon^2)\, E_c\, I_\varepsilon .$$

From these normalized equations it is seen that for any given set of inputs, the output of the standard Western Electric transistor is about 11 times as large as the output of the modified, padded General Electric transistor.

by first varying the applied signal, then adjusting the padding resistance in similar direction, and finally analyzing the distortion frequency component at the output for gains and distortions.

Comparison Between Results of Types 11 and 1-1698

For comparing the behavior and range of multiplication between the two proposed transistor components, both the graphical presentation of Figures 7 and 12 and the equations (2) and (3) will be utilized. For ready reference, these equations are:

$$I_c = (0.548 - 0.0377 V_e^2 - 0.328 I_3^2) V_e I_3 \qquad (2)$$

for the alloyed junction transistor, Type 2N[illegible], [illegible],

$$\text{and } I_c = (1.025 + 0.0092 V_e^2 - 0.0885 I_3^2) V_e I_3 \qquad (3)$$

for the grown diffused junction transistor, General Electric, Type 11 transistor.

Normalizing these equations with respect to the input product yields for equation (2)

$$\frac{I_c}{[illegible]} = (1 + 0.1105 V_e^2 - 1.0 I_3^2) V_e I_3,$$

and for equation (3)

$$\frac{I_c}{[illegible]} = (1 + 0.0090 V_e^2 - 0.0863 I_3^2) V_e I_3.$$

From these normalized equations it is seen that for any [illegible] the [illegible] multiplication [illegible] it comes at input on the [illegible] of the multiplier [illegible] General Electric transistor,

Of more importance however; the error portions of the output of the standard Western Electric transistor are 17.2 and 33.9 times as large as the corresponding error portions of the equivalent General Electric transistor.

Arbitrarily considering a maximum acceptable error of 5 percent, Figures V and VII show that the range of possible input values for the equivalent General Electric transistor is about four times that of the standard Western Electric transistor.

From these considerations it is evident, that for the chosen operating point, the modified, padded General Electric transistor offers greater possibilities for utilization in practical multiplication circuits.

Response as a Function of Frequency

The results of the frequency investigation of the modified, padded General Electric transistor are best analyzed from Figure XII. From an inspection of these curves it is concluded that as the mean of the input frequencies is increased, the accuracy falls off slightly until a frequency of about 4,000 cps is reached. At about this frequency accuracy starts to improve. The optimum of accuracy is reached at about 6,000 or 7,000 cps. Upon further increase in the mean of the input frequencies, the accuracy of multiplication is radically reduced. It is therefore concluded that accuracy sets an upper

limit on the input frequencies of about 10,000 cps. This places a severe frequency limitation upon the possible use of this equivalent transistor as an electronic multiplying device.

Response as a Function of Temperature

In certain applications the frequency limitation may not be critical. Because of this, a further investigation of the effect of temperature variations upon the equivalent transistor response is recommended.

Interchangeability

Finally, an investigation is recommended to determine the interchangeability of transistors; that is, the variation of multiplicative characteristics among several transistors of the same type.

V. APPENDIX

A. DETAILS OF PROCEDURE

Preliminary Procedure

An attempt was initially made to check the transistor's adaptability to electronic multiplication by mathematical analysis of the usually accepted linear equivalent circuit. This approach proved useless since multiplication is essentially a nonlinear operation which obviously could not be derived from a linear equivalent circuit. An attempt was then made to determine the transistor's adaptability to the problem by a combination mathematical and graphical analysis of the transistor characteristics as published by the manufacturer. No definite conclusion could be reached by this method because of the infinite number of possible choices as to operating points and amplitudes of sinusoidal inputs. Further, the accuracy of this type of analysis was very poor due to inherent graphical inaccuracies. This became particularly apparent when small sinusoidal inputs were considered.

It was then decided to investigate the problem primarily by experimental methods and subsequently attempt to correlate the experimental findings with the transistor characteristics.

Type A-1698 Investigation with Direct Inputs

An experimental investigation of the application of an

unpadded Western Electric, Type A-1698, transistor was made. Direct current and voltage inputs were first used. The results were again inconclusive primarily because of measurement difficulties. The incremental d-c values to be measured were so small with respect to the bias values that accuracy of measurement was not possible even after balancing out a fixed portion of the bias.

Type A-1698 Investigation with One Alternating Input

In an attempt to circumscribe this difficulty the unpadded transistor was driven with a direct emitter current input and a biased sinusoidal collector voltage input. The a-c signal in the output current could then be isolated by blocking the d-c path with a capacitor whose impedance to the a-c signal was negligible. The results of this experiment were heartening. With a properly biased a-c signal, an output current proportional, within 5 percent, to the product of the d-c and a-c inputs was obtained. However a very high attenuation between the true product of the inputs and the measured output was experienced. These results can be explained by reference to Figure 1 on page 9 . Perfect multiplication will result if, in the area of operation, the slopes of the constant i_ε curves are inversely proportional to the values of i_ε, and the curves of constant i_ε are straight lines at arbitrary horizontal spacing.

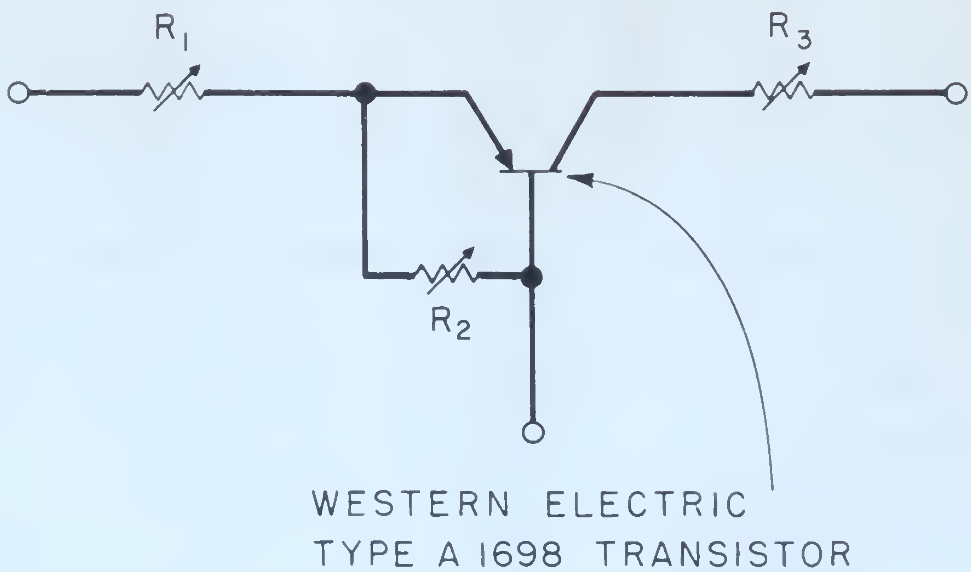
This investigation indicated that there was a restricted area over which these stipulations held within plus or minus 5 percent. Though this experiment was encouraging it provided a very limited solution to the general problem of multiplication. For this reason no further investigation from this viewpoint was attempted.

Resistive Padding of Type A-1698

From a study of the desired characteristics as discussed on page 10 of the procedure it was decided to attempt to improve the standard transistor characteristics. To accomplish this the resistive network of Figure XIII was added to form another equivalent transistor. Through adjustment of the resistors R_1, R_2 and R_3, it was hoped to attain perfect multiplication over at least a limited range of inputs. Unfortunately this work on the Western Electric transistor, padded as shown in Figure XIII, failed to produce the desired results. The linearity of the constant i_ε curves could be improved, or the horizontal spacing of these curves could be made more nearly equal. However, one of these results could be accomplished only by a serious forfeiture of the other. An attempt to determine a set of optimum values for the padding resistors (R_1, R_2, and R_3) was not made at this juncture because it was decided that it would be more desirable to make a comparison between the multiplicative

FIGURE XIII

EQUIVALENT PADDED TRANSISTOR



ability of a standard transistor and that of one with reduced point-contact pressure and adjusted padding resistors.

Approximate Adjustment of Padding Resistors Shown in Figure II

The qualitative effects of changes in the values of the padding resistors shown in Figure II on page 14 was assessed by means of a plotter that automatically traced the collector characteristics. An approximate adjustment was made for optimum radial linearity and equal horizontal spacing. These values were: $R_1 = 200\Omega$, $R_2 = 1.6K$, $R_3 = 19K$.

Static Characteristics

Through use of the circuit of Figure III, page 14, with the a-c generators short circuited, an attempt was made to measure the static collector characteristics for various values of the padding resistors. This proved impossible because the quantity measured depended upon the direction from which it was approached. This phenomenon was attributed primarily to moisture effects. These effects had been aggravated because the transistor had been opened for lightening. A typical discrepancy obtained when varying i_ε from zero to four ma and back to zero was a 25 percent difference in the i_c readings between the first and second zero of i_ε.

Linearity Check

To determine the effect on radial linearity due to changes in the padding resistors, the following scheme was first tried. At a given operating point, i_ε was held constant and an alternating signal (E_c) of known amplitude was applied. The alternating component of collector current (I_c) was measured. If the constant i_ε curves were to be linear, it follows that I_c should be proportional to E_c. Even though it had been observed on the plotter that changes in the padding resistors had marked effect on the linearity, it proved very difficult to discern these effects when utilizing this scheme.

A second method was tried which proved quite satisfactory. Emitter current was again held constant, but instead of keeping the operating point fixed and varying E_c, E_c was held constant and the operating point was moved up and down the constant i_ε curve. If the curves were to be linear, it follows that I_c should be constant. Around the operating point of $E_{co} = -4$ volts and $I_{\varepsilon o} = 1.5$ ma, the optimum linearity adjustment yielded $R_1 = 200\Omega$, $R_2 = 2K$, and $R_3 = 10K$.

Horizontal Spacing Check

To check the horizontal spacing a constant amplitude, alternating signal (I_ε) was applied to the emitter. The operating point was moved along a constant e_c line. The

alternating component of collector current was measured. If the horizontal spacing was to be equal, i_c should be constant. A consideration from this point of view yielded optimum values of $R_1 = 400\Omega$, $R_2 = 750\Omega$, and $R_3 = 5K$.

Linearity with these values was checked. Since the linearity was not greatly different from that obtained with the optimum for linearity, whereas changes in the resistors had a critical effect on spacing, it was decided to use these last values for the succeeding work.

Collector Characteristics

Sufficient data had been taken when determining spacing and linearity to plot the collector characteristics of the modified, padded transistor. For information this is shown in Figure XIV.

Taylor Series Expansion

$$I_c = f(e_c, i_\varepsilon)$$

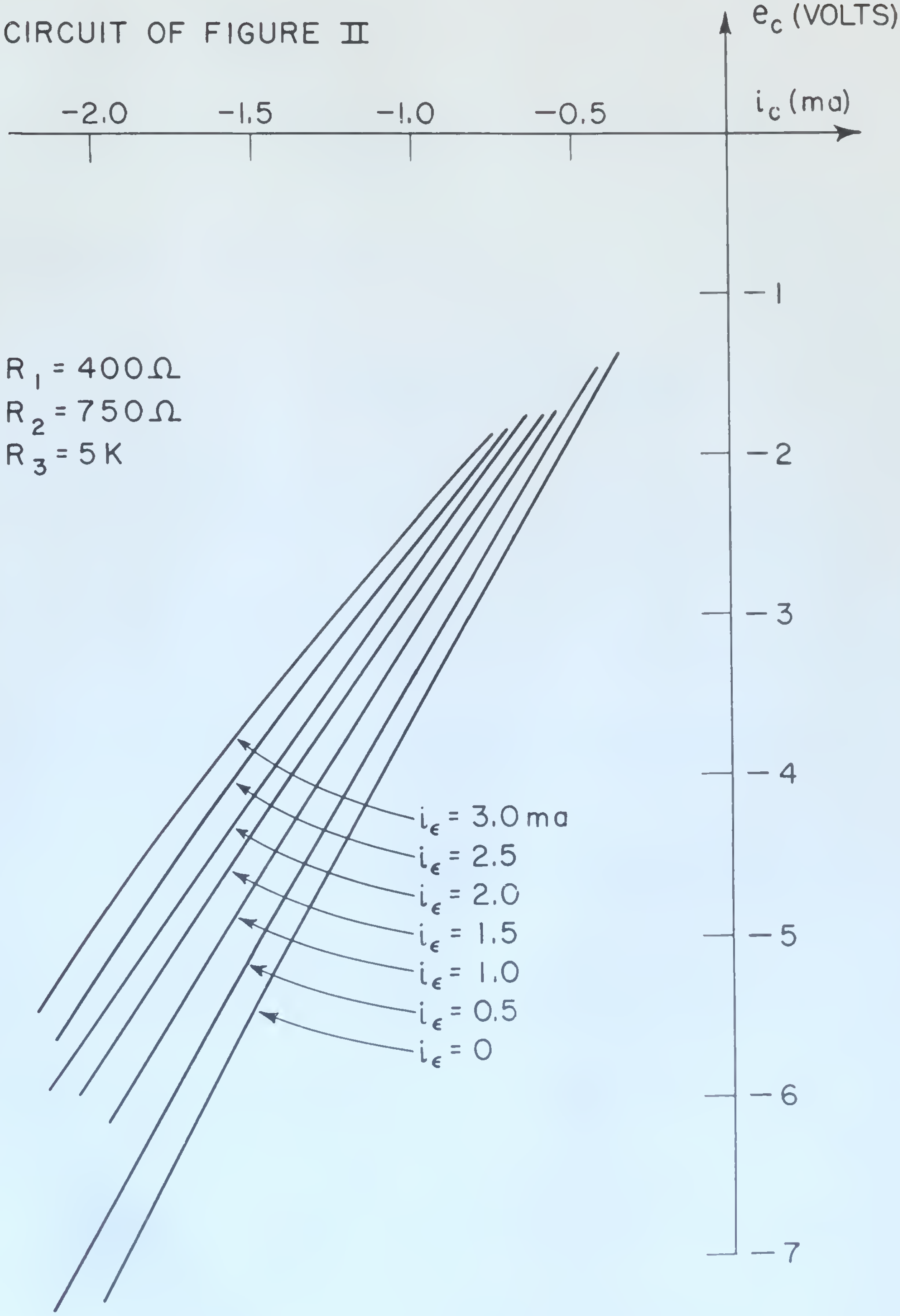
When expanded the nth term is

$$\left[\frac{1}{(n-1)!}\left\{(e_c - E_{co})\frac{\partial}{\partial e_c} + (i_\varepsilon - I_{\varepsilon o})\frac{\partial}{\partial i_\varepsilon}\right\}^{n-1} f(e_c, i_\varepsilon)\right]_{\substack{e_c = E_{co} \\ i_\varepsilon = I_{\varepsilon o}}}$$

$$i_c = f(E_{co}, I_{\varepsilon o}) + (e_c - E_{co})\frac{\partial f(E_{co}, I_{\varepsilon o})}{\partial e_c} + (i_\varepsilon - I_{\varepsilon o})\frac{\partial f(E_{co}, I_{\varepsilon o})}{\partial i_\varepsilon} +$$

FIGURE XIV

COLLECTOR CHARACTERISTICS OF PADDED TRANSITOR MARCH 17, 1952 S. N. R.



$$\frac{1}{2}\left[(e_c - E_{co})^2 \frac{\partial^2 f(E_{co}, I_{\varepsilon o})}{\partial e_c^2} + 2(e_c - E_{co})(i_\varepsilon - I_{\varepsilon o}) \frac{\partial^2 f(E_{co}, I_{\varepsilon o})}{\partial i_\varepsilon \partial e_c} +\right.$$

$$\left.(i_\varepsilon - I_{\varepsilon o}) \frac{\partial^2 f(E_{co}, I_{\varepsilon o})}{\partial i_\varepsilon^2}\right] +$$

$$1/6 \left[(e_c - E_{co})^3 \frac{\partial^3 f(E_{co}, I_{\varepsilon o})}{\partial e_c^3} + 3(e_c - E_{co})^2 (i_\varepsilon - I_{\varepsilon o})\right.$$

$$\frac{\partial^2 f(E_{co}, I_{\varepsilon o})}{\partial e_c^2} \frac{\partial f(E_{co}, I_{\varepsilon o})}{\partial i_\varepsilon} +$$

$$3(e_c - E_{co})(i_\varepsilon - I_{\varepsilon o})^2 \frac{\partial f(E_{co}, I_{\varepsilon o})}{\partial e_c} \frac{\partial^2 f(E_{co}, I_{\varepsilon o})}{\partial i_\varepsilon^2} +$$

$$\left.(i_\varepsilon - I_{\varepsilon o})3 \frac{\partial^3 f(E_{co}, I_{\varepsilon o})}{\partial e_c^3}\right] +$$

$$1/24 \left[(e_c - E_{co})^4 \frac{\partial^4 f(E_{co}, I_{\varepsilon o})}{\partial e_c^4} +\right.$$

$$4(e_c - E_{co})^3 (i_\varepsilon - I_{\varepsilon o}) \frac{\partial^3 f(E_{co}, I_{\varepsilon o})}{\partial e_c^3} \frac{\partial f(E_{co}, I_{\varepsilon o})}{\partial i_\varepsilon} +$$

$$6(e_c - E_{co})^2 (i_\varepsilon - I_{\varepsilon o})^2 \frac{\partial^2 f(E_{co}, I_{\varepsilon o})}{\partial e_c^2} \frac{\partial^2 f(E_{co}, I_{\varepsilon o})}{\partial i_\varepsilon^2} +$$

$$4(e_c - E_{co})(i_\varepsilon - I_{\varepsilon o})^3 \frac{\partial f(E_{co}, I_{\varepsilon o})}{\partial e_c} \frac{\partial^3 f(E_{co}, I_{\varepsilon o})}{\partial i_\varepsilon^3} +$$

$$\left.(i_\varepsilon - I_{\varepsilon o})^4 \frac{\partial^4 f(E_{co}, I_{\varepsilon o})}{\partial i_\varepsilon^4}\right] + \cdots\cdots$$

Since the partial derivatives at a particular operating point are constant, the notation may be simplified by writing them as b's with subscripts. If the excursions from the operating point are sinusoidal we can write the following expressions:

$$e_c - E_{co} = E_{cm}\sin\omega_1 t$$

$$i_\epsilon - I_{\epsilon o} = I_{\epsilon m}\sin(\omega_2 t+\psi)$$

$$i_c = b_1 + b_2 E_{cm}\sin\omega_1 t + b_3 I_{\epsilon m}\sin(\omega_2 t+\psi)$$

$$+ \tfrac{1}{2}\Big[b_4 E_{cm}^2\sin^2\omega_1 t + 2b_5 E_{cm} I_{\epsilon m}\sin\omega_1 t\sin(\omega_2 t+\psi)$$

$$+ b_6 I_{\epsilon m}^2\sin^2(\omega_2 t+\psi)\Big]$$

$$+ 1/6\Big[b_7 E_{cm}^3\sin^3\omega_1 t + 3b_8 E_{cm}^2 I_{\epsilon m}\sin^2\omega_1 t\sin(\omega_2 t+\psi)$$

$$+ 3b_9 E_{cm} I_{\epsilon m}^2\sin\omega_1 t\sin^2(\omega_2 t+\psi) + b_{10} I_{\epsilon m}^3\sin^3(\omega_2 t+\psi)\Big]$$

$$+ 1/24\Big[b_{11} E_{cm}^4\sin^4\omega_1 t + 4b_{12} E_{cm}^3 I_{\epsilon m}\sin^3\omega_1 t\sin(\omega_2 t+\psi)$$

$$+ 6b_{13} E_{cm}^2 I_{\epsilon m}^2\sin^2\omega_1 t\sin^2(\omega_2 t+\psi) + 4b_{14} E_{cm} I_{\epsilon m}^3\sin\omega_1 t$$

$$\sin^3(\omega_2 t+\psi) + b_{15} I_{\epsilon m}^4\sin^4(\omega_2 t+\psi)\Big] + \dots$$

If the appropriate trigonometric substitutions are made, there is obtained:

$$i_c = b_1 + b_2 E_{cm}\sin\omega_1 t + b_3 I_{\epsilon m}\sin(\omega_2 t+\psi)$$

$$+ \tfrac{1}{2}\Big[b_4 E_{cm}^2\tfrac{1}{2}(1-\cos 2\omega_1 t) + 2b_5 E_{cm} I_{\epsilon m}\big(-\tfrac{1}{2}\cos\{(\omega_1+\omega_2)t+\psi\}$$

$$+ \tfrac{1}{2}\cos\{(\omega_1-\omega_2)t-\psi\}\big) + b_6 I_{\epsilon m}^2\tfrac{1}{2}(1-\cos\{2\omega_2 t+2\psi\})\Big]$$

$$+ 1/6\Big[b_7 E_{cm}^3\tfrac{1}{2}(3/2\sin\omega_1 t - \tfrac{1}{2}\sin 3\omega_1 t) + 3b_8 E_{cm}^2 I_{\epsilon m}\tfrac{1}{2}$$

$$(\sin\{\omega_2 t+\psi\} - \tfrac{1}{2}\sin\{(2\omega_1+\omega_2)t+\psi\} - \tfrac{1}{2}\sin\{(\omega_2-2\omega_1)t+\psi\}) +$$

$$3b_9 E_{cm} I_{\epsilon m}^{2} \tfrac{1}{2}\left(\sin \omega_1 t - \tfrac{1}{2}\sin\left\{(2\omega_2 + \omega_1)t + 2\psi\right\}\right.$$

$$\left. - \tfrac{1}{2}\sin\left\{(\omega_1 - 2\omega_2)t - 2\psi\right\}\right) + b_{10} I_{\epsilon m}^{3} \tfrac{1}{2}\left(3/2 \sin(\omega_2 t + \psi)\right.$$

$$\left. - \tfrac{1}{2}\sin(3\omega_2 t + 3\psi)\right\}\Big] +$$

$$1/24\Big[b_{11} E_{cm}^{4} \tfrac{1}{2}(3/2 - 2\cos 2\omega_1 t + \cos 4\omega_1 t) +$$

$$4b_{12} E_{cm}^{3} I_{\epsilon m} \tfrac{1}{2}\left(-3/4 \cos\left\{(\omega_1 + \omega_2)t + \psi\right\} +\right.$$

$$3/4 \cos\left\{(\omega_1 - \omega_2)t - \psi\right\} + \tfrac{1}{4}\cos\left\{(3\omega_1 + \omega_2)t + \psi\right\}$$

$$\left. - \tfrac{1}{4}\cos\left\{(3\omega_1 - \omega_2)t - \psi\right\}\right)$$

$$+ 6b_{13} E_{cm}^{2} I_{\epsilon m}^{2} \tfrac{1}{2}\left(1 + \tfrac{1}{2}\cos\left\{2(\omega_1 + \omega_2)t + 2\psi\right\} +\right.$$

$$\left. \tfrac{1}{2}\cos\left\{2(\omega_1 - \omega_2)t - \psi\right\} - \cos 2\omega_1 t - \cos\left\{2\omega_2 t + 2\psi\right\}\right) +$$

$$4b_{14} E_{cm} I_{\epsilon m}^{3} \tfrac{1}{2}\left(-3/4 \cos\left\{(\omega_1 + \omega_2)t + \psi\right\} + 3/4 \cos\left\{(\omega_1 - \omega_2)t - \psi\right\} +\right.$$

$$\left. \tfrac{1}{4}\cos\left\{(3\omega_2 + \omega_1)t + 3\psi\right\} - \tfrac{1}{4}\cos\left\{(3\omega_2 - \omega_1)t + 3\psi\right\}\right) +$$

$$b_{15} I_{\epsilon m}^{4} \tfrac{1}{2}\left(3/2 - 2\cos(2\omega_2 t + 2\psi) + \cos\left\{4\omega_2 t + 4\psi\right\}\right)\Big] + \cdots \quad (4)$$

It is seen from the above that the output contains the following difference frequency term:

$$i_{c\,\substack{\text{diff.}\\ \text{freq.}}} = \left[\tfrac{1}{2} b_5 E_{cm} I_{\epsilon m} + 1/16\, b_{12} E_{cm}^{3} I_{\epsilon m} + 1/16\, b_{14} E_{cm} I_{\epsilon m}^{3} + \cdots\cdots\right] \cos\left\{(\omega_1 - \omega_2)t - \psi\right\} \quad (5)$$

In order to simplify future calculations, this equation can be rewritten using rms values.

$$I_{c\,\substack{\text{diff.}\\ \text{freq.}}} = a_5 E_c I_\epsilon + a_{12} E_c^{3} I_\epsilon + a_{14} E_c I_\epsilon^{3} + \cdots\cdots \quad (6)$$

B. SAMPLE CALCULATIONS

a_5

This coefficient can be calculated from the plotted results shown in Figure V on page 17 and Figure VII on page 20. Equation (6) on page 42 gives the expression for the difference frequency output current that was measured. From Figure VII, it is seen that for relatively small signals there is no measurable discrepancy from perfect multiplication. Therefore in this range the error terms can be neglected, and a_5 can be calculated from a direct substitution of values.

At $E_c = 1.0$ v

and $I_\epsilon = 0.9$ ma

$I_c = 0.0261$ is read.

Therefore $0.0261 = a_5\,(1.0)\,(0.9)$

or $a_5 = 0.029$.

a_{12}

Differentiating equation (6) with respect to E_c yields:

$$\frac{\partial I_c}{\partial E_c} = a_5 I_\epsilon + a_{14} I_\epsilon^3 + 3a_{12} E_c^2 I_\epsilon \qquad (7)$$

By examining any constant I_ϵ curve of Figure VII it is seen that the derivative of I_c with respect to E_c decreases for increasing values of E_c. It then follows from equation (7) that a_{12} is negative.

From examination of equation (4) on page 42, it is seen that the magnitude of a_{12} can be calculated from the measured value at the $(3\omega_1 + \omega_2)$ frequency.

Measured value $\frac{16}{24}(4)\, a_{12} E_c^3 I_\varepsilon (\frac{1}{2})(\frac{1}{4})$

or measured value $= \frac{1}{3} a_{12} E_c^3 I_\varepsilon$

For $E_c = 2.0$ volts; $I_\varepsilon = 1.04$ ma; measurement $= 0.00054$ ma.

Therefore $a_{12} = \frac{(0.00054)\ (3)}{(8)\ (1.04)} = 0.000195$

For $E_c = 2.5$ volts; $I_\varepsilon = 1.25$ ma; measurement $= 0.00134$ ma.

Therefore $a_{12} = \frac{(0.00134)\ (3)}{(15.6)\ (1.25)} = 0.000206$

For $E_c = 2.5$ volts; $I_\varepsilon = 1.562$ ma; measurement $= 0.0016$ ma.

Therefore $a_{12} = \frac{(0.0016)\ (3)}{(15.6)\ (1.25)} = 0.000197$

Therefore a_{12} was taken equal to 0.0002.

<u>a_{14}</u>

Differentiating equation (6) with respect to I_ε yields:

$$\frac{\partial I_c}{\partial I_\varepsilon} = a_5 E_c + a_{12} E_c^3 + 3a_{14}' E_c I_\varepsilon^2 \qquad ([illegible])$$

By examining Figure VIII, which is a cross plot of Figure VII, it is seen that the derivative of I_c with respect to I_ε decreases for increasing values of I_ε. This indicates from equation ([illegible]) that a_{14} is also negative.

Similar to the a_{12} calculations, a_{14} can be calculated from the measured value at the $(3\omega_2 - \omega_1)$ frequency.

Measured value $= \frac{16}{24}(4)\, a_{14}\, E_c\, I_\varepsilon^3 \left(\frac{1}{2}\right)\left(\frac{1}{4}\right)$

or measured value $= \frac{1}{3}\, a_{14}\, E_c\, I_\varepsilon^3$

For E_c = 2.0 volts; I_ε = 1.04 ma; measurement = 0.00061 ma.

Therefore $a_{14} = \frac{(0.00061)\,(3)}{(2)\,(1.13)} = 0.00081$

For E_c = 2.5 volts; I_ε = 1.25 ma; measurement = 0.0013 ma.

Therefore $a_{14} = \frac{(0.0013)\,(3)}{(2.5)\,(1.95)} = 0.0008$

For E_c = 2.5 volts; I_ε = 1.562 ma; measurement = 0.0025 ma.

Therefore $a_{14} = \frac{(0.0025)\,(3)}{(2.5)\,(3.82)} = 0.000786$

Therefore a_{14} was taken equal to 0.0008.

C. ORIGINAL DATA

Western Electric, Type A1698. Circuit Diagram, Figure IV

E_{co} = -4 volts, $I_{\varepsilon o}$ = 1.5 ma, I_{co} = 5.38 ma.

April 15, 1952.

$E_{I\varepsilon}$-450 cps across 1K	E_c-350 cps	E_{Ic}-100cps across 750Ω	E_{Ic}-1500cps across 750Ω	E_{Ic}-1000 cps across 750Ω
50 mv	500 mv	6.0 mv	Not measured	Not measured
	750	8.6	"	"
	1000	10.7	"	"
	1250	12.5	"	"
	1500	13.5	1.4 mv	"
	2000	13.[illegible]	3.4	"
100	500	11.4	Not measured	Not measured
	750	16.5	"	"
	1000	21.0	"	"
	1250	25.0	"	"
	1500	27.0	2.8	0.13 mv
	2000	27.5	6.8	0.17
150	500	17.2	Not measured	Not measured
	750	24.8	"	"
	1000	31	"	"
	1250	36	"	"
	1500	40	4.3	0.44
	2000	40	10.0	0.59
200	500	22	Not measured	Not measured
	750	32	"	"
	1000	40	"	"
	1250	47	"	"
	1500	51	5.7	1.0
	2000	52	13.5	1.4

General Electric padded, modified transistor.

Circuit Diagram, Figure III

$E_{co}=-4$ volts, $I_{\varepsilon o}=1.5$ ma.

April 4, 1952

$E_{1\varepsilon}$-450 cps across 9.0Ω	E_c-350 cps	E_{1c}-100cps across 100Ω	E_{1c}-1500 cps across 100Ω	E_{1c}-1000 cps across 100Ω
1 volt	0.5 volts	0.15 mv	Too small to read	Too small to read
1	1.0	0.29	"	"
1	1.25	0.36	"	"
1	2.0	0.58	"	"
1	2.5	0.67	"	"
2	0.5	0.30	"	"
2	1.0	0.595	Not measured	Not measured
2	1.5	0.92	"	"
2	2.0	1.20	"	"
2	2.5	1.43	"	"
2	2.8	1.57	"	"
4	0.5	.615	"	"
4	1.0	1.21	"	"
4	1.5	1.83	"	"
4	2.0	2.41	"	"
4	2.5	2.94	"	"
4	2.8	3.20	"	"
6	0.5	0.94	"	"
6	1.0	1.82	"	"
6	1.5	2.60	"	"
6	2.0	3.65	"	"
6	2.5	4.40	"	"
6	2.8	4.75	"	"
8.65	0.5	1.31	"	"
8.65	1.0	2.62	"	"
8.65	1.5	3.90	"	"
8.65	2.0	5.00	"	"
8.65	2.5	5.90	"	"
10.0	2.0	5.40	0.054 mv	0.061 mv
12.0	2.5	7.60	0.134	0.13
15.0	2.5	8.60	0.160	0.25

General Electric padded, modified transistor.

Circuit Diagram, Figure III

V_{co}=-4 volts, I_{Eo}=1.5 ma.

April 25, 1952.

ω_1	ω_2	V_{I_E} across 9.6	V_c	V_{I_c} diff. freq. across 100Ω
350 cps	450 cps	2 volts	0.5 volts	.305 mv
			1.0	.605
			1.5	.910
			2.0	1.195
			2.5	1.42
		4	0.5	.610
			1.0	1.20
			1.5	1.80
			2.0	2.39
			2.5	2.93
3.5 kc	4.0 kc	2	0.5	.283
			1.0	.562
			1.5	.945
			2.0	1.10
			2.5	1.31
		4	0.5	.569
			1.0	1.12
			1.5	1.69
			2.0	2.23
			2.5	2.74
6.75 kc	7.25 kc	2	1.0	.505
		4	1.0	.794
9.75 kc	10.25 kc	2	1.0	.434
		4	1.0	.885
15.5 kc	16 kc	2	0.5	.126
			1.0	.250
			1.5	.376
			2.0	.494
			2.5	.506
		4	0.5	.335
			1.0	.661
			1.5	.990
			2.0	1.30
			2.5	1.57

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